CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An image sensor comprising:

a photosensor including a charge collection region of a first conductivity type located within a substrate; and

an implanted region of a second conductivity type, said implanted region being located laterally of said photosensor and adjacent said charge collection region.

2. The image sensor of claim 1, wherein said photosensor is a photodiode.

3. The image sensor of claim 2, wherein said photodiode is an n-p photodiode.

4. The image sensor of claim 2, wherein said photodiode is a p-n photodiode.

5. The image sensor of claim 2, wherein said photodiode is a p-n-p photodiode.

6. The image sensor of claim 2, wherein said photodiode is an n-p-n photodiode.

7. The image sensor of claim 1, wherein said photosensor is a photogate.

8. The image sensor of claim 1, wherein said photosensor is a photoconductor.

9. The image sensor of claim 1, further comprising a gate structure of a transistor formed over said substrate, at least a portion of the bottom of said gate structure being in contact with said implanted region.

10. The image sensor of claim 9, wherein said gate structure comprises a transfer transistor gate for transferring charge accumulated in said charge collection region to a floating diffusion region of said first conductivity type.

11. The image sensor of claim 9, wherein said gate structure is a reset gate.

12. The image sensor of claim 1, wherein said implanted region has a thickness of about 0.5 microns to about 7.0 microns.

13. The image sensor of claim 12, wherein said implanted region has a thickness of about 1.0 microns to about 5.0 microns.

14. The image sensor of claim 1, wherein said implanted region is doped with a p-type dopant at a dopant concentration of from about 1×10^{16} to about 1×10^{17} atoms per cm^3.

15. The image sensor of claim 14, wherein said implanted region is doped with a p-type dopant at a dopant

concentration of about 5 x10^{15} to about 5 x10^{16} atoms per cm^3.

16. The image sensor of claim 1, wherein said first conductivity type is p-type and said second conductivity type is n-type.

17. The image sensor of claim 1, wherein said first conductivity type is n-type and said second conductivity type is p-type.

18. A photosensor for use in an imaging device, said photosensor comprising:

a first doped layer of a first conductivity type formed in a substrate;

a charge collection region formed in said first doped layer for accumulating photo-generated charge, said charge collection region being of a second conductivity type and being laterally adjacent an implanted region of said first conductivity type; and

a second doped layer of said first conductivity type formed in said first doped layer and above said charge collection region.

19. The photosensor of claim 18, wherein said photosensor is a photodiode.

20. The photosensor of claim 19, wherein said photodiode is an n-p photodiode.

21. The photosensor of claim 19, wherein said photodiode is a p-n photodiode.

22. The photosensor of claim 19, wherein said photodiode is a p-n-p photodiode.

23. The photosensor of claim 19, wherein said photodiode is an n-p-n photodiode.

24. The photosensor of claim 18, wherein said photosensor is a photogate.

25. The photosensor of claim 18, wherein said photosensor is a photoconductor.

26. The photosensor of claim 18, wherein said implanted region is in contact with said charge collection region.

27. The photosensor of claim 18 further comprising a gate of a transistor formed over said substrate, at least a portion of the bottom of said gate being in contact with said implanted region.

28. The photosensor of claim 27, wherein said gate is a reset gate.

29. The photosensor of claim 18 further comprising a transfer gate of a transfer transistor adjacent said charge collection region, said transfer gate transferring charge accumulated in said charge collection region to a doped region of said second conductivity type.

30. The photosensor of claim 18, wherein said implanted region is doped with a p-type dopant at a dopant concentration of from about 1 x 10^{16} to about 1 x 10^{17} atoms per cm^3.

31. The photosensor of claim 30, wherein said implanted region is doped with a p-type dopant at a dopant concentration of about 5 x10^{15} to about 5 x10^{16} atoms per cm^3.

32. The photosensor of claim 18, wherein said implanted region has a thickness of about 0.5 microns to about 7.0 microns.

33. The photosensor of claim 32, wherein said implanted region has a thickness of about 1.0 microns to about 5.0 microns.

34. The photosensor of claim 18, wherein said first conductivity type is p-type and said second conductivity type is n-type.

35. The photosensor of claim 18, wherein said first conductivity type is n-type and said second conductivity type is p-type.

36. An image sensor comprising:

a silicon substrate;

a shallow trench isolation region formed within said silicon substrate;

a pixel within an area at least partially defined by said shallow trench isolation region and comprising a photosensor, said photosensor further comprising a p-type pinned layer and an n-type doped layer located adjacent and below said p-type pinned layer;

a channel region of an adjacent transistor; and

a p-type implanted region adjacent said n-type doped layer and said channel region.

37. The image sensor of claim 36, wherein said photosensor is part of a 3T pixel cell.

38. The image sensor of claim 36, wherein said photosensor is part of a 4T pixel cell.

39. The image sensor of claim 36, wherein said transistor is a transfer transistor.

40. The image sensor of claim 36, wherein said transistor is a reset transistor.

41. The image sensor of claim 36, wherein said p-type implanted region is located along at least a portion of the bottom of said channel region.

42. The image sensor of claim 36, wherein said n-type doped region is a floating diffusion region.

43. The image sensor of claim 36, wherein said p-type implanted region has a thickness of about 0.5 microns to about 7.0 microns.

44. The image sensor of claim 43, wherein said p-type implanted region has a thickness of about 1.0 microns to about 5.0 microns.

45. The image sensor of claim 36, wherein said p-type implanted region has a dopant concentration of from about 1×10^{16} to about 1×10^{17} atoms per cm^3.

46. The image sensor of claim 45, wherein said p-type implanted region has a dopant concentration of about $5x10^{15}$ to about $5 x10^{16}$ atoms per cm^3.

47. An image sensor comprising:

a silicon substrate;

a shallow trench isolation region formed within said silicon substrate;

a pixel within an area at least partially defined by said shallow trench isolation region and comprising a photosensor;

a channel region of an adjacent transistor; and

an implanted region adjacent said photosensor and said channel region.

48. The image sensor of claim 47, wherein said photosensor is a photodiode.

49. The image sensor of claim 48, wherein said photodiode is a p-n-p photodiode, said p-n-p photodiode further comprising a p-type pinned layer and an n-type doped layer located adjacent and below said p-type pinned layer.

50. The image sensor of claim 47, wherein said transistor is a transfer transistor, said transfer transistor transferring charge accumulated in said n-type doped layer to another n-type doped region.

51. The image sensor of claim 50, wherein said n-type doped region is a floating diffusion region.

52. The image sensor of claim 47, wherein said implanted region is a p-type implanted region located along at least a portion of the bottom of said channel region.

53. The image sensor of claim 52, wherein said p-type implanted region has a thickness of about 0.5 microns to about 7.0 microns.

54. The image sensor of claim 53, wherein said p-type implanted region has a thickness of about 1.0 microns to about 5.0 microns.

55. The image sensor of claim 47, wherein said implanted region has a dopant concentration of from about 1 x 10^{16} to about 1 x 10^{17} atoms per cm^3.

56. The image sensor of claim 55, wherein said implanted region has a dopant concentration of about 5x10^{15} to about 5 x10^{16} atoms per cm^3.

57. An image sensor comprising:

a silicon substrate;

a shallow trench isolation region formed within said silicon substrate;

a pixel within an area at least partially defined by said shallow trench isolation region and comprising a p-n-p photodiode, said p-n-p photodiode further comprising a p-type pinned layer and an n-type doped layer located adjacent and below said p-type pinned layer;

a channel region of a transfer transistor, said transfer transistor transferring charge accumulated in said n-type doped layer to another n-type doped region; and

a p-type implanted region adjacent said n-type doped layer and said channel region.

58. The image sensor of claim 57, wherein said p-type implanted region is located along at least a portion of the bottom of said channel region.

59. The image sensor of claim 57, wherein said n-type doped region is a floating diffusion region.

60. The image sensor of claim 57, wherein said p-type implanted region has a thickness of about 0.5 microns to about 7.0 microns.

61. The image sensor of claim 60, wherein said p-type implanted region has a thickness of about 1.0 microns to about 5.0 microns.

62. The image sensor of claim 57, wherein said p-type implanted region has a dopant concentration of from about 1×10^{16} to about 1×10^{17} atoms per cm^3.

63. The image sensor of claim 62, wherein said p-type implanted region has a dopant concentration of about $5x10^{15}$ to about $5 x10^{16}$ atoms per cm^3.

64. An imager system comprising:

a processor; and

an imaging device coupled to said processor, said imaging device comprising:

an isolation region formed in a substrate;

a pixel adjacent said isolation region, said pixel comprising a photosensor adjacent a gate structure of a transistor, said photosensor further comprising a layer of said first

conductivity type, and a doped region of a second conductivity type located below said layer; and

an implanted region of said first conductivity type laterally and adjacent said photosensor, and in contact with said doped region.

65. The system of claim 64, wherein said implanted region has a thickness of about 0.5 microns to about 7.0 microns.

66. The system of claim 65, wherein said implanted region has a thickness of about 1.0 microns to about 5.0 microns.

67. The system of claim 64, wherein said first conductivity type is p-type and said second conductivity type is n-type.

68. The system of claim 64, wherein said first conductivity type is n-type and said second conductivity type is p-type.

69. The system of claim 64, wherein said photosensor is a photodiode.

70. The system of claim 69, wherein said photodiode is an n-p photodiode.

71. The system of claim 69, wherein said photodiode is a p-n photodiode.

72. The system of claim 69, wherein said photodiode is an n-p-n photodiode.

73. The system of claim 69, wherein said photodiode is a p-n-p photodiode.

74. The system of claim 64, wherein said photosensor is a photogate.

75. The system of claim 64, wherein said photosensor is a photoconductor.

76. The system of claim 64, wherein said gate is a transfer gate for transferring charge accumulated in said doped region of said second conductivity type to a floating diffusion region of said second conductivity type, said floating diffusion region being opposite said doped region.

77. The system of claim 64, wherein said gate is a reset gate.

78. A method of forming a photosensor of a pixel cell, said method comprising:

forming a first doped layer of a first conductivity type in said substrate;

forming a doped region of a second conductivity type in said first doped layer and between a gate structure and an isolation region; and

forming an implanted region of said first conductivity type in said substrate, said implanted region being lateral of and in contact with said doped region.

79. The method of claim 78, wherein said implanted region is formed along at least a portion of the bottom of said gate structure.

80. The method of claim 78, wherein said implanted region is formed by implanting a p-type dopant below at least a portion of said gate structure.

81. The method of claim 78, wherein said implanted region is doped with a p-type dopant at a dopant concentration of about 1 x 10^{16} to about 1 x 10^{17} atoms per cm^3.

82. The method of claim 81, wherein said implanted region is doped with a p-type dopant at a dopant concentration of about 5 x10^{15} to about 5 x10^{16} atoms per cm^3.

83. The method of claim 78, wherein said implanted region is formed to a thickness of about 0.5 microns to about 7.0 microns.

84. The method of claim 83, wherein said implanted region is formed to a thickness of about 1.0 microns to about 5.0 microns.

85. The method of claim 78, wherein said act of forming said implanted region further comprises forming a photoresist layer over said gate structure and said substrate, and patterning and etching said photoresist layer to expose an area of said substrate located between said isolation region and said doped region.

86. The method of claim 85 further comprising the act of implanting a p-type dopant below said area of said substrate.

87. The method of claim 86 further comprising forming a second doped layer of said first conductivity type in said substrate and above said doped region.

88. The method of claim 78, wherein said photosensor is a photodiode.

89. The method of claim 88, wherein said photodiode is an n-p photodiode.

90. The method of claim 88, wherein said photodiode is a p-n photodiode.

91. The method of claim 88, wherein said photodiode is a p-n-p photodiode.

92. The method of claim 88, wherein said photodiode is an n-p-n photodiode.

93. The method of claim 78, wherein said photosensor is a photogate.

94. The method of claim 78, wherein said photosensor is a photoconductor.

95. The method of claim 78, wherein said gate structure is a transfer gate.

96. The method of claim 78, wherein said gate structure is a reset gate.

97. A method of forming a photosensor for an imaging device, said method comprising:

forming a gate of a transistor over a silicon substrate;

forming a first p-type doped layer in said silicon substrate;

forming an n-type doped region below said first p-type doped layer; and

forming a doped region lateral of and in contact with said n-type doped region by implanting p-type ions below at least a portion of said gate and within an implant area of said silicon substrate, said doped region having a dopant concentration within the range of from about 1×10^{16} to about 1×10^{17} atoms per cm^3.

98. The method of claim 97, wherein said doped region is formed along at least a portion of the bottom of said gate.

99. The method of claim 97, wherein said gate is a transfer gate of a transfer transistor.

100. The method of claim 97, wherein said gate is a reset gate of a reset transistor.

101. The method of claim 97, wherein said doped region is formed to a thickness of about 0.5 microns to about 7.0 microns.

102. The method of claim 101, wherein said doped region is formed to a thickness of about 1.0 microns to about 5.0 microns.

103. The method of claim 97, wherein said act of forming said doped region further comprises forming a photoresist layer over said gate and said substrate, and patterning and etching said photoresist layer to expose said implant area of said substrate.

104. The method of claim 103 further comprising the act of forming said implant area between said isolation region and said n-type doped region.

105. The method of claim 104 further comprising the act of implanting a p-type dopant below said implant area of said substrate.

106. A method of forming a barrier implanted region within a channel region of a transistor, said method comprising:

forming a gate structure of a transistor over a substrate;

forming source and drain regions of a first conductivity type on opposite sides of said gate structure, said source and drain regions forming a channel region within said substrate and between said source and drain regions; and

forming a barrier implanted region of a second conductivity type within said channel region and adjacent said gate

structure, said barrier implanted region having a barrier dopant concentration higher than the substrate dopant concentration.

107. The method of claim 106, wherein said barrier implanted region is formed by implanting ions below at least a portion of said gate and within said substrate.

108. The method of claim 106, wherein said barrier implanted region has a dopant concentration within the range of from about 1 x 10^{16} to about 1 x 10^{17} atoms per cm^3.

109. The method of claim 108, wherein said barrier implanted region has a dopant concentration of about 5 x10^{15} to about 5 x10^{16} atoms per cm^3.

110. The method of claim 106, further comprising the step of forming a charge collection region of said first conductivity type lateral of and adjacent said barrier implanted region.

111. The method of claim 106, wherein said gate structure is a transfer gate.

112. The method of claim 106, wherein said gate structure is a reset gate.